2D Intelligent Pulsed Light Source Technology in 2D Neutron Detector Performance Calibration System

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Abstract

China Spallation Neutron Source (CSNS) Project will use a batch of 2D neutron detectors that are based on ZnS (Ag) scintillators doped with 6Li. To ensure the application consistency of these neutron detectors, a 2D neutron detector performance calibration system is developed. Considering the radiation safety problem, direct experiment with large-scale radioactive particles is inconvenient. Therefore, the following scheme is designed: an equivalent photon producing system where neutron bombardment of scintillators is replaced by motion scanning of controlled pulsed laser light source in the 2D mobile platform. The kernel of the control system in the calibration system is the core controller that is based on the embedded system STM32 and the FPGA chip. The controller interfaces with the PC computer and receives commands via TCP/IP to generate the intelligent pulse signal with adjustable frequency, duty ratio and amplitude. The pulse signal controls LD laser to generate pulsed light source signal. The pulsed light source is placed in the 2D mobile platform controlled by the core controller, and the calibration medium is introduced through the optical fiber. The PC computer receives the electronic unit signal in the calibration system and performs data processing to automatically calibrate the performance parameters of 2D detectors. The experimental results show that the pulse signal source satisfies the requirements of 2D neutron detector performance calibration system.

Keywords: CSNS, 2D neutron detector, Pulsed Light Source, FPGA chip, Calibration System.

1. INTRODUCTION

China Spallation Neutron Source (CSNS) Project is located in Dalang Town, Dongguan City. Its first phase will be completed in 2018, by which a number of accelerators and spectrometers will be built (China Spallation Neutron Source project, 2016). Subsequently, an additional 15 spectrometers will be built. High-performance neutron detector is a key device in the neutron scattering experiment, and the majority of traditional neutron scattering spectrometers use high-pressure 3He gas detector (Chen and Wang, 2016). However, in the recent 20 years, the price of 3He gas has risen more than 20 times; moreover, its supply has become increasingly difficult in recent years. In view of this, CSNS will use a batch of 2D neutron detectors that are based on 6LiF/ZnS (Ag) scintillators (Wu et al., 2013). To ensure the application consistency of these neutron detectors, a 2D neutron detector performance calibration system is developed. For radiation safety, the control of radioactive sources is becoming increasingly stringent in China, so direct experiment with large-scale radioactive particles is inconvenient. Therefore, design of an equivalent neutron beam system is needed for calibrating the performance of neutron detectors.

2. 2D neutron detectors and calibration method

2.1 Composition and principle of neutron detectors

Figure 1 illustrates the schematic diagram of the scintillator detectors
Scintillator (6LiF/ZnS (Ag)) is a neutron-sensitive material, so when neutrons hit it, the following nuclear reactions will occur on its surface (Yang et al., 2015):

\[ ^{4}\text{He}^{6}\text{Li} \rightarrow ^{1}\text{H}(2.72\text{MeV}) + ^{4}\text{He}(2.05\text{MeV}) \]

Two types of particles on the right side of the above reaction equation produce photons under ionization excitation, thereby emitting isotropic light. As the scintillators are opaque, the light reaching the scintillators is absorbed. Another part of light arrives at the wavelength shift fiber (WLSF) array and is absorbed by WLSF (Dongol et al., 2016). The emission spectrum of photons is shown by the green line in Figure 2a, which highly coincides with the absorption spectrum (black line) of WLSF at 380-450 nm. WLSF collects the scintillation light and transmits it to the multi-anode photomultiplier (MA-PMT) (Photomultiplier). The WLSF emission spectrum (red line) is in the range of 480-550 nm, which coincides with the MA-PMT response spectrum (shown in Figure 2b). Thus, WLSF plays a role in the coupling of photons to the MA-PMT. After photoelectric conversion through MA-PMT, the output electrical signal enters the electronic board and read out by the simplified circuit. Back-end circuit is responsible for the amplification, filtering, shaping, discrimination, triggering and counting of signals. Then, the signals are transmitted to the data acquisition system via the point-to-point interface and processed by the PC (Sun et al., 2010), as shown in Figure 1.

The key performance indicators of detector unit are shown in Table 1:

<table>
<thead>
<tr>
<th>No</th>
<th>Main technical parameters</th>
<th>Parameter indicator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Effective detection area of the detector unit</td>
<td>200mm×450mm</td>
</tr>
<tr>
<td>2</td>
<td>Diameter of WLSF</td>
<td>1mm</td>
</tr>
<tr>
<td>3</td>
<td>Spatial resolution</td>
<td>&lt;5mm×50mm</td>
</tr>
<tr>
<td>4</td>
<td>Thermal neutron detection efficiency</td>
<td>&lt;5mm×50mm</td>
</tr>
<tr>
<td>5</td>
<td>Total count rate</td>
<td>&gt;30 kHz</td>
</tr>
<tr>
<td>6</td>
<td>Electronics Time Measurement Accuracy</td>
<td>&lt;1µs</td>
</tr>
</tbody>
</table>
2.2 Composition of calibration system's control system

For incident particles of given energy and scintillation screen of fixed dimension, the size of excitation beam spots, photon yield and distribution of emitted photons are relatively fixed. If the WLSF is slightly damaged during wiring, the transmission attenuation of photons will also differ greatly. Influenced by the manufacturing process, the transmission gain difference of PMT components can often reach one order of magnitude. Therefore, for the unit performance parameters of scintillator detectors, the step responsible for their fluctuations is primarily the WLSF to PMT gain. Therefore, the function needing to be completed by the automatic calibration system is: calibration of the part consisting of the photon transmission to MA-PMT via LSF and the electrical signal output after MA-PMT photoelectric conversion. To complete the calibration task, signal source is required. So, it is necessary to design a set of simulated 2D light sources to simulate the photons generated by interaction between neutrons and scintillation screen.

The structure of the automatic calibration system is shown in Figure 3. Its working principle is as follows:

![Figure 3 Automatic Calibration System Chart](image)

According to Table 1 and Figure 2, the performance requirements on pulsed light source are as follows:

Wavelength requirements on pulsed light source: 380-450 nm.

Temporal requirements on pulsed light source: temporal resolution $>10$ ns; frequency $>30$ kHz; and error $>0.1\%$ within 100 kHz working frequency.

Amplitude requirements on pulsed light source: adjustable; resolution $>0.1\%$; and error $>1\%$.

Motion control accuracy of 2D mobile platform: better than 0.1 mm.

2.3 Design of controller system

As the kernel of calibration system, the overall system architecture of the controller is shown in Figure 4.
The controller comprises embedded system, FPGA, pulse signal output interface, 2D mobile platform (XY platform) control interface and TCP/IP interface.

Pulse signal output circuit: ARM transmits the computing cycle and the number of clocks corresponding to pulse width to the FPGA. FPGA then generates the cycle- and pulse width-adjustable pulse signal (P1) and controls the 12-bit DAC chip DAC8512 to generate the amplitude-variable analog signal (V1). P1 and V1 are connected to the ADG741 high-speed analog switch as the input end, whose output is the pulse electrical signal (V2) with adjustable frequency, pulse width and amplitude. After filtering (V3), the signal controls the LD laser to produce 405 nm pulsed light source.

2D mobile platform (XY platform) control interface: motor is controlled by FPGA-based stepper motor driver DM442, while SIKO magnetic scale MSK5000 is used as the sensor. The sensor-feedback signal is collected by the FPGA to form the closed-loop control of 2D mobile platform.

3. XY platform control system

ARM, the core of control system, receives commands from the host PC and gives the target motion position, i.e. the given value in the figure. It also uses magnetic scale as the position sensor to feedback the positional information of the controlled target slider for directional judgment and counting by FPGA. ARM makes judgments and determines the modes of motion by reading the positional information through FPGA (including the status of limit switch), which also connects to the stepper motor driver DM442 by outputting the pulse, direction and enable signals through FPGA. The driver DM442 controls the stepper motor.

3.1 XY platform drive unit

1) DM442 interface signal

Digital stepper motor driver DM442 (Dong et al., 2014) integrates the functions of sequential pulse generation and power drive. The external interface input only requires the pulse, direction and enable signals, whereas the output directly drives the stepper motor, as shown in Figure 5a. All the three signals are differential signals, namely:

Pulse signal PUL: PUL+, PUL-

Direction signal DIR: DIR+, DIR-

Enable signal ENA: ENA+, ENA-

2) Limit switch interface signal

Limit switch is installed at the edge of XY platform. If the edge position has been reached, relevant message should be sent instantly, and the motor movement must be stopped immediately to avoid any accident. Such a component is precisely the limit switch. There is a total of four limit switches, which are responsible for the detection of top-end positions in the two directions, respectively. The interface circuit is shown in Figure 5b. When the switch does not work, the output signal is at high level; and when it moves, the signal is at low level.
3) ARM and FPGA interfacing circuit

FGGA is the buffer between STM32F407 (Zhang and Zhao, 2011) (Nagy et al., 2014) and the external signal interface. As shown in Figure 6, the STM32F407's embedded FSMC interface writes the FSMC’s FIFO to the FPGA through the 16-bit bus data [15, 0], wrrep, rdreq, clock, FPGA-CS0, FPGA-NADV, FPGA-NWAIT and FSMC-CLK clock and control signals.

4) Stepper motor drive circuit

Programming of the signal generation circuit for differential output signals PUL, DIR and ENA is completed in FPGA. STM32F407 (ARM) receives the PC commands to identify the moving target value and determines the number of DIR, ENA and PUL pulses through the magnetic scale and limit feedback signal.

There are three differential signals PUL, DIR, ENA in the FPGA and in each step motor driver DM442 interface, while two DM442 (each in X, Y directions) have 6 signals. Among them, PUL+, DIR+, ENA+ are all 5 V, whereas PUL-, DIR-, ENA- are output to the driver DM442 by the output of FPGA (level 3.3 V) through the triode open collector circuit (MC1413, with 7 units). The driving principle is shown in Figure 7. The figure presents the schematic diagram of one signal, and that for the remaining five signals are similar.

5) Design of FPGA interface program

FPGA programming is completed in the quartus ii development environment. Quartus ii is a comprehensive PLD/FPGA development software from Altera. It supports a variety of input forms and provides a series of FPGA chip design models, which is capable of completing the entire PLD design flow from design input to hardware configuration. The Verilog HDL programming language is used in the FPGA system to realize the interface design of stepper motor driver.

3.2 Feedback signal processing
Sensor outputs two digital signals with the non-contact SIKO magnetic scale MSK5000 (Zhuang and Zhang, 2013). Its primary performance parameters are as follows:

1) Supply voltage: 5V±5%, in line with the system's supply voltage.

2) Output signal: A, B square signals, with a phase difference of 90°.

3) Resolution: 0.005 mm.

4) Inherent error:

$$\Delta L = \pm (0.025 + 0.01 \times L) \text{ mm}$$

Where: L is the measuring span, unit: m

As the long side of 2D platform is 0.5 m in length, $\Delta L$ maximum error: ±0.03 mm, which meets the system requirements.

As shown in Figure 7, the sensor output signals are: A, B square signals. W in the figure represents a cycle, which is in a forward state in the first half, and in a reverse state in the second half.

![Figure 7](image1)

**Figure 7** The sensor output signal waveform figure

![Figure 8](image2)

**Figure 8** Sensor signal filter circuit

Taking into account the jittering of platform during movement, there will be jamming signals during signal transmission, so filter circuit is installed to filter out spikes. Figure 9 presents the RC filter circuit, where the capacitor selection has taken into account the highest signal frequency factor. Since FPGA chip has a 3.3V power supply and the sensor has a 5 V power supply, the circuit is also equipped with partial pressure function for matching the interface level.

The A and B signals output from the sensor are fed into the FPGA through the RC filter circuit. FPGA first undergoes signal shaping, and then enters the square signal detector for detection and recording of signals A and B, thereby obtaining the speed, direction and position feedback information of the stepper motor. RTL view of the feedback circuit is shown in Figure 9 below:
Simulation of the feedback circuit can yield the following results, as shown in Figure 10:

Simulation results analysis:

1) rst_n: circuit reset signal;

2) sys_clk: system clock with a frequency of 50 MHz;

3) A, B: output square signals of analog sensor, which are the feedback input signal;

4) DIR: This pin represents the feedback outputs in the forward and reverse motor rotating directions. If the level is high, it indicates that the motor is rotating in the forward direction. If the level is low, it indicates that the motor is rotating in the reverse direction. The parameter changes with changing phase difference between A and B signals.

5) POSITION: position output of the stepper motor. If the motor is running forward, the position counter will be incremented by 1 upon detection of a square wave from sensor. If the motor is running reverse, the counter will be decremented by 1 upon detection of a square wave.

3.3 Implementation of control system

The circuit board adopts a 4-layer PCB board structure: 2 layers are the power supply and ground planes, while the other 2 layers are signal line tracing planes. Signal layer and power plane are arranged at intervals. This greatly lowers the noises of power and ground signals while reducing crosstalk between signals.

As the entire board is mixed analog-digital circuit, particular attention should be paid to suppress the digital circuit's interference to the analog part. The handling method includes the following points:

1) Domain separation: make sure that the analog and digital circuits are not mixed.

2) Independency of power supplies: make sure that the power supplies for the analog and digital parts are not commonly grounded, which are only connected at the "root" of power supplies. This greatly ensures that the analog power supply is unaffected by the digital circuit. A major principle is that the ground loop current of digital circuit should not pass through the analog circuit part.
3) To ensure that the circuit is not damaged due to short circuit overcurrent, self-recovering fuse is connected to each power input end. When the current is too large, and temperature rises, the fuse will be disconnected for protection. After temperature recovery, the fuse can continue to work.

The program is written based on ucos II embedded real-time operating system. When the system is running, all functional functions are subject to the scheduling management of the operating system, so the engineering codes must all satisfy the "dispatchable" basic principle. In addition, all function realization functions are present in the form of "tasks". Each task has a unique priority, and the referential basis for system task scheduling order is the exclusive and unique priority of each task.

4 TEST RESULTS AND APPLICATION

4.1 Test results

1) Pulse signal source test

After multiple experiments, the results obtained by setting different amplitude parameters of host PC interface and using the actual output voltages of DAC measured with high-precision voltmeter exhibit a relative full-scale error of 0.125% at maximum compared to the PC default value, which is better than the design error of 1%.

Pulse signal source has a temporal resolution of 2.5 ns, which is better than the system measurement requirements of 10 ns. The frequency of pulse signal is set by the host PC, and output frequency is measured with high-precision frequency meter. The maximum error is revealed to be 0.025% in the range below 100 kHz, which is better than the requirement of 0.1%

2) XY platform performance testing

After repeated tests, the control system's positioning errors are all within ±0.02 mm according to the reading of magnetic scale. The system accuracy of magnetic scale: Maximum error: ±0.03 mm. The overall error of XY platform is within ±0.05 mm, which meets the design error requirements of 0.1 mm.

4.2 Formation of pulse light source

The optical module uses 405 nm programmable semiconductor laser as the light source. The laser operates in continuous mode, which adjusts the output power in real time by the output pulse signal of the control system; modulates the appropriate optical pulses; and finally projects them onto the WLSF with optical fiber.

Maximum output power of laser is 120mW; drain output power is 0.12mW; and maximum allowable frequency of modulation analog signal 1MHz. The laser output energy is much higher than the normal incidence of scintillator detectors, so attenuation is required. The purpose of attenuation, on the other hand, is to let the WLSF get the incident photon number close to that under the working conditions of scintillator detectors; and on the other hand, is to suppress the drain output power and to reduce the number of background incident photons. Concerning the attenuation modulation, laser intensity is attenuated step by step to avoid the excessively large laser power from damaging the components. Meanwhile, multiple output paths can be separated in the optical circuit to facilitate the monitoring of laser pulses.

Figure 11 shows the diagram of scheme for laser intensity attenuation modulation. Since there will be some delay in the interval from laser reception of control signals to emission of laser pulses, direct use of laser controlling electrical signal as a trigger is not very accurate. Monitor1 APD is used to detect the laser pulse as the temporal trigger signal. Monitor2 PMT is used to assist in recording the intensity of laser pulses, which can also be used as a trigger for laser pulses instead of Monitor1 APD. In the right-most optical fiber adapter in Figure 11, the laser is divided into two by the optical fiber adapter, and the output intensity ratio between the two parts is fixed. By detecting the intensity of laser pulses on the Monitor2 PMT, the intensity contrast value for laser pulses irradiated on the array of scintillator position-sensitive nuclear detector fiber can be obtained, which can be used as a scale in the efficiency measurements (since simulation of light output resulting from neutron nuclear reaction within the scintillators is required, the laser pulses impinging on the fiber array need to be modulated, so that the number of photons reaches the nominal level, which is consistent with the light output...
of neutron nuclear reaction). SC-PMT0 is a photomultiplier coupled to the array of the scintillator position-sensitive detector fiber, which is a signal readout component of the scintillator detector.

Figure 11 Attenuating modulation scheme of laser intensity

5. CONCLUSION

The development of two-dimensional neutron detector performance calibration system has been applied in the "fast neutron detection and electronic technology" joint laboratory (cooperation in the establishment by Dongguan Institute of Technology and the Institute of High Energy Physics), the application indicates that the system meets the test requirements.

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