A Smart Cascade Interface Chip for Piezoelectric Sensor

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Abstract
A novel generic architecture for piezoelectric sensor interface chip is presented in the paper, which makes it possible to cascade interface chip to prove its performance, and relieve the limitations of integration processes, cost, size and other factors to chip performance, greatly expand the application of this sensor interface chip. This chip has channel, analog to digital converter (ADC), memory three kinds of cascade models in order to meet the different test requirements for sampling frequency, acquisition channel and storage capacity. The design approach achieved automatic control of the cascade chips by using programming of cascade model and parameter, host-slave controlling and status recognition. The chip is carried out in a standard 0.18 \textmu m CMOS process. Experiments and applications show the chip based on this developed generic architecture has excellent performance in application for different kinds of dynamical parameters.

Key words: Sensor Interface, Generic Architecture, Cascade, Piezoelectric Sensor.

1. INTRODUCTION
Miniature storage measurement systems (MSMS) have been widely used for acquiring dynamical signals (such as acceleration/pressure) in the field of armaments, aeronautics & astronautics, petroleum exploration, etc. (Bissi and Placidi, 2007; Pennisi, 2005), which have two characters, one is that MSMS can be embedded in the body of be tested object, the other is that the input signals of MSMS have very extended rang of dynamical characters.

Miniaturization and low power consumption are the main features of MSMS (Ebrahim and Mohamad, 2007). These can be realized by interface circuit integrated (Bracke and Merken, 2005; Darko and Bojan, 2014). Traditionally, most of this sensor interfaces must be tailored towards a specific application (Ricardo and Katayoun, 2014). This leads to a narrow application range. When the test conditions and environment changes, the existing interface-chips may not meet the test requirements. But, re-designing will bring high costs and a very long time. So, the major challenge of design is how to extend the applications range of interface chip.

In previous studies, several research groups expand the application range of the interface chip by constituted generic architectures (Baschirotto and Capone, 2008). Some embedded configurable blocks in the interface chips which are similar to the FPGA or CPLD, and can be programmed (Arvinda and Pramananda, 2016; Rachana and Hitesh, 2016; Leong and Semiao, 2015). Some is dividing many sub-scales of offset and gain (Bracke and Merken, 2005) to attach different input signals. These generic architectures can adjust the performance parameters within limits for matching the input signal, but they can only use for single interface chip and which versatility will be restrictions on chip performance.

The input signals of MSMS are dynamic parameters which bandwidth or duration time maybe variance at the power of 2 or 3. MSMS only relay on the generic architectures above mentioned can’t meet the test request of different type dynamic parameters. Therefore, it’s necessary to develop a new generic architecture of integrated interface chip.

In this paper, a smart cascade interface chip (SCIC) is presented, which architecture can break to the limited of chip itself through some interface chips cascade and can raise the performances of the MSMS timely. The limited of chip itself not only refers to the performances have been designed and reality, but also point to the integrated technique and optimization design. This cascade method has the advantage of highly integrated, low connectivity, without external control devices and so on, compared with cascade of merchant chip. It can also be the same as other generic architectures, through the programming to choose their operating parameters.
This paper is organized as followings: a multisensor microsystem based on this novel cascade interface chip has been introduced in chapter 2, Chapter 3 presents the design and implementation of cascade function, Chapter 4 describes the application and experiment results and Chapter 5 concludes the paper.

2. SYSTEM ARCHITECTURE WITH SCIC

The microsystem based on SCIC consists of piezoelectric sensors, oscillator, one or more SCIC and rechargeable battery (see Fig.1). SCIC has four operation modes: no cascade mode, channel cascade, ADC cascade and memory cascade. The operation mode can be preselected according to the characters of input signals.

![Figure 1 Microsystem architecture with smart cascade interface chip or chips](image1)

2.1 Architecture of SCIC

Generally, sensor of MSMS is piezoelectric, so the type of input signal of SCIC is charge. As shown in Fig.2, the analog signals (charge) produced by the sensors are amplified and filtered in SCIC, then transferred to the ADC. The digital data from ADC are written into memory at real time. When measurement finished, data transferred to PC from communication interface through special cable. The system’s operation has been under the control of system control unit and cascade control unit.

![Figure 2 Proposed SCIC block diagram](image2)

Restrictions on the application of interface chip depend primarily on the signal range, bandwidth and duration, storage capacity and other factors. Placed the relevant resistors, capacitors outside the interface chip can be easily and quickly achieve the adjustment of input range. Adopt the method of selected the sampling frequency by programming and chip cascading and so on, effectively extends the range of bandwidth, duration, the required storage capacity and other parameters of the measured signal.

2.2 The Expansion of the range of Measured Signal

SCIC has four analog signal input channels, which range determined by sensitivity of sensor and feedback capacitance of Charge Amplifier (CA). CA acts as a charge to voltage converter and amplifier for the input signal.

The relations between feedback capacitance $C$ of CA, sensitivity $k$ of sensor and scale $S$ of system are as follows:

$$ u = -\frac{Sk}{C} (1) $$

Where $u$ is the output voltage of CA, its range is determined by the reference voltage of the ADC. When the sensor is selected, $S$ from the $C$ value of the decision, that is, choose a different $C$ values can be different from the measurement range.
The filter in SCIC is second-order voltage-controlled voltage source of low-pass filter which is the most commonly type for MSMS, its cutoff frequency \( f \) determined by the resistance values of \( R_f \) and capacitor \( C_f \) of filter circuit (shown as Eq.(2)).

\[
f = \frac{1}{2\pi R_f C_f}
\]  

(2)

So, the feedback capacitance of CA and the capacitance, resistance of filter has to be mounted outside of the chip for flexible replacement to enhance the generic of SCIC.

### 2.3 The Expansion of the Type of Measured Signal

The bandwidth, duration, required storage capacity and other parameters with the measured signals of different types will appear very different, thus becoming the main factor limited chip’s applications. To single SCIC, the Nyquist criteria, stating that the sampling frequency should be at least twice higher than the maximum frequency appearing in the signal to be sampled, is the basis of the sampling rate choice. The measured signals of different bandwidth should choose the appropriate sampling frequency, which not only can avoid aliasing and noise problems, but also can avoid a large number of redundant data storage to cause the waste of memory. The sampling frequency of ADC can be chosen by programming with frequency range: from 5 kHz to 1MHz in SCIC. If a higher sampling frequency is needed, can be a few pieces of the AD cascade model of SCICs achieved. For a longer duration signals, if when selecting the appropriate sampling frequency, the chip’s storage capacity still cannot meet their needs, we can cascade several SCICs in memory cascade model for expansion of storage capacity.

In addition, we can also connect several SCICs in channel cascade model to meet the needs of multi-parameter testing at the same time.

### 3. CASCADE ARCHITECTURES DESIGN

In cascade mode, firstly, the SCICs connect each other with some relative pins and form parallel or serial topological structure. Secondly, they need to be programmed for selecting which operation mode or parameters (such as sampling frequency) according to the requirement of application respectively.

### 3.1 Programming and Configuration of Cascade SCIC

A programming enable pin has been set in each SCIC. When this pin is in valid state, the SCIC can be programmed on virtual panel and configured through special cable. Tab.1. shows the relationship between programming information and configuration bits.

<table>
<thead>
<tr>
<th>Selected</th>
<th>Programmable options</th>
<th>Configuration bits</th>
<th>value</th>
<th>function</th>
</tr>
</thead>
<tbody>
<tr>
<td>operation mode</td>
<td>Cascade mode</td>
<td>PE1 PE0</td>
<td>00</td>
<td>no cascade</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>ADC cascade</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>memory cascade</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>channel cascade</td>
</tr>
<tr>
<td>Operation and data reading order</td>
<td>PE3 PE2</td>
<td>00</td>
<td>First</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>Second</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>Third</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>Fourth</td>
</tr>
<tr>
<td>Number of cascade</td>
<td>PE5 PE4</td>
<td>00</td>
<td>One</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>Two</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>Three</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>Four</td>
</tr>
<tr>
<td>operation parameters</td>
<td>Sampling frequency</td>
<td>PE8 PE7PE6</td>
<td>000</td>
<td>1Mps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001</td>
<td>500ksps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010</td>
<td>200ksps</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>011</td>
<td>100ksps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>50ksps</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>101</td>
<td>20ksps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110</td>
<td>10ksps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111</td>
<td>5ksps</td>
</tr>
<tr>
<td>Trigger mode</td>
<td>PE9</td>
<td></td>
<td>0</td>
<td>Out trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Inner trigger</td>
</tr>
</tbody>
</table>

SCIC has different operation modes and parameters, in which, operation modes including whether cascade or not, how to cascade; operation parameters have nothing to do with the cascade, including the sampling...
frequency and trigger modes and so on. These can enhance the flexibility and applicability of system because of independent assortment of different operation modes and parameters.

The value of Configuration bits is decided by the user’s programming information. For example, when user select “ADC cascade” operation mode from virtual panel, (PE1, PE0) equals (00) then transferred to SCIC from special cable. The two bits control the circuit operated according to the request of ADC operation mode. Whatever select which cascade mode, the operation and data reading order must be programmed, otherwise, which can lead to working confusedly and data collision.

3.2 Design and Realization of Cascade Modes

Only no cascade mode need one SCIC, else need more SCICs (at most four) connect with each other by a few relative pins. These chips have different topological structures in different modes (see Fig.3):

- Channel cascade: Cascade SCICs have parallel structure, which sample and store the respective input dynastic parameters of the measured object in the same test course at the same time.
- Memory cascade: In this mode, SCICs store the data one by one according to the order programmed with serial structure.
- ADC cascade: MSMS is consisted of cascade SCICs can improve system sample rate in ADC cascade mode. These SCICs circularly operated, i.e. which are with circular serial structure.

![Figure 3 Topological structure of cascade SCICs in different modes](image)

$$p_e = n \cdot p_s (3)$$

Eq.3 shows the relation of performance between cascade SCICs—pc and single SCIC—ps, where n is the number of cascade SCICs. pc and ps may be the quantity of channels, size of memory or sampling rate. This novel configuration can break through the limit of chip and enable the system acquire higher performance.

The architectures of SCIIC is shown in Figure 4, which not only have the varied operation parameters similar to the generic architectures mentioned before, but also have the cascade function to extend the measurement rang.

Configuration bits transfer into SCIIC through the pin of TRX. The two pins SEL1, SEL2 act as the controller of cascade, in case of cascade, the two pins of all cascade chips’ connect respectively. They are bi-directional pins, which direction is effectively designed by the value of PE3 PE2. The SCIIC named master-chip when it’s (PE3 PE2) = (00) and it’s SEL1, SEL2 are output-direction; others are slave-chip whose pins are input-direction.

1. Operation of no cascade mode

In this mode, the system needs one SCIIC. The clock CLK1 is divided by frequency selected then formed sampling clock CWE with frequency range: from 5 kHz to 1MHz in the SCIIC. Users can select appropriate sampling frequency according to bandwidth of input signal and Nyquis for avoiding abundance redundant data. The operation parameters which can select by programming also include trigger mode, time of delay, value of trigger voltage, etc. These parameters can be programmed in cascade mode also.

2. Operation of ADC cascade

Some dynamic signal with very sharp rising edge, but the ADC’s sampling frequency of SCIIC is limited to 1MHz in SCIIC. We can get higher sampling frequency in ADC cascade mode and unnecessarily redesign. The system’s sampling frequency is n times higher than no cascade mode, the value of n equals to the quantity of cascade SCIICs.
If system needs 4MHz sampling frequency, we can connect four SCICs together. The system clock clk_vcry is input in every SCIC with the frequency of 4MHz, signal should be sampled at every rising edge of that.

In each SCIC, the input clock clk_vcry is processed by the block of Divided and shifted and Clock selected (see Fig.4), and then formed the clock SWE. The sampling clock WE of SCIC is the same as SWE in ADC cascade mode. At first, clock clk_vcry input and produced four clocks: clk1, clk2, clk3 and clk4 by frequency divided and shifted, the four clocks have same frequency 1MHz but different phases. Next, select one from the four clock and turn into sampling clock of this SCIC (clock SWE) according to the chip’s programmed operation order, i.e. the value of (PE3 PE2):

① If (PE3 PE2) equals (00), clk1 is selected and turn into sampling clock SWE of this SCIC.
② If (PE3 PE2) equals (01), clk2 is outputted and turned into the clock SWE of this SCIC.
③ If (PE3 PE2) equals (10), clk3 is selected and output.
④ If (PE3 PE2) equals (11), the sampling clock SWE of this SCIC comes from clk4.

Each SCIC samples the signal at the falling edge of respective SWE. Thus, at every rising edge of clk_vcry, there must be a SCIC which is sampling signal (see Fig.5). That is the SCIC of cascade system operated circularly and orderly in ADC cascade mode. Although each SCIC samples with 1MHz, the system based on four SCICs can sample with 4MHz.

(3) Operation of memory cascade

When the quantity of sampled data goes beyond the memory size of SCIC, memory cascade is needed. The cascade SCICs sample at the same time, but storage data at chronological sequence, one is written full, the next one continue, until all of them are full, which order is also determined by the value of PE3PE2.
The key of this operation mode is how to realize the cascade SCICs operated orderly and continuous. The pins SEL1 SEL2 take on the task, through which mast-chip outputs the message of chip selected to every cascade SCIC continuously.

The effectiveness of the operation of memory depends on the following three factors (shown in Fig.4):

a) The value of (PE1 PE0): This value determines whether the validity of memory operations with the output of the block of Chip selected. If (PE1 PE0) is equal to (10), which signified SCIC operated in memory cascade mode, the validity decided by it, else has nothing to do with it.

b) Output of the block of Chip selected: When (PE1 PE0)=(10) and the output of this block CS is high level, the clock of write (WE1) or read (OE) can input to memory. In every chip, only when the two values of (SEL1 SEL2) and (PE3 PE2) are complete equality, CS can be as high level.

c) SCIS’s current work status: Whether allows the memory to read or write operation is decided by the state variables TC. The clock WE1 which frequency is the same as clock WE is the write clock of memory. The clock OE is reading clock of memory, which sent out from PC. In order to reduce the power consumption of system, the oscillator is shut off when sampling is finished (at the moment state variable TC=1). When TC=0, clock WE1 can input in memory and permit data wrote in.

In master-chip, WE1 is counted by counter during sampling, so long as the quantity reaches 512k (memory size is 512k in each chip), the value of SEL1 SEL2 are added and outputted to every chip. The value of configuration bits PE5, PE4 are inputted to counter for ascertaining the number of cascade chips. When all the memory of chips is written fully, the sampling course is finished and the value of state variable TC changes from 0 to 1 at the same time. Then, chips are turned into waiting-transfer-data state automatically. Because (PE3PE2)=(00) in master-chip, so the data is always the first to write in. Fig. 6 shows the simulation waveform of master-chip in memory cascade mode. From that, we can see that the course of white and read are began from master-chip. When the value of SEL1 SEL2 is changed, the course finished (reference Figure 4).

In slave-chip, the block of Chip selected has always compared the value of (SEL1 SEL2) with (PE3 PE2). Only these two values are same, the chip is able to write the current data into its own internal memory. When in cascade mode, the SCIC has the advantage of less external lead, high reliability, without external control chip and so on compared with the commodity chips, because each one integrated ADC, memory and controllers.

(4) Operation mode of channel cascade

Some generic measurements such as Waveform Recorder are able to be cascaded when number of channels is less than number of measured parameters. SCIC has the same function, in some cases it can be cascaded to measure lots of parameters at one time.

In this mode, SCICs operated in parallel and every chip must be programmed order in order to transferred data intense and accurately. In sampling course, every chip samples at same time. But the order of transfer data is different according to the value of CS. The operation of master-chip is shown in Figure 7.
3.3 Data Readout of Cascaded Chips

Finished measurement (TC=1), system should be connected to PC for data transfer. Command of read data is produced by virtual panel when user decides to begin. Memory is controlled under the Write and read clock selected block.

When (PE1PE0) equals (00), system is in no cascade mode (see Tab.1 and Fig.4). The read clock OE input to memory from Write and read clock selected block to control data transfer. In this condition, the output of this block has irrelevant to else input signals.

When (PE1PE0) doesn’t equal (00), representing more SCICs consist a system, so, data should be read out from one SCIC then another. In these cascade SCICs, whether the read clock OE can input to memory is related to the signal CS and the value of TC. Memory operated in this course resembles the sampling course in memory mode.

4. IMPLEMENTATION AND APPLICATION OF SCIC

The SCIC is designed in a 0.18 μm CMOS technology for a supply voltage between 2.7 and 3.3V with size of 7mm × 8mm (see Fig.8). The size of internal SRAM is 512k × 12bit. In no cascade mode, the power consumption is 24.6mW (3V, 8.2mA) at on-state.

The build-in ADC (see Fig.9) is successive approximation type, which accuracy is 12 bits. The sampling rate of the ADC is chosen, range from 5 kHz to 1MHz. It has been tested with 5kHz sin wave signal. The results based on FFT analysis is shown in table 2:

<table>
<thead>
<tr>
<th>SINAD</th>
<th>ENOB</th>
<th>INL</th>
<th>DNL</th>
</tr>
</thead>
<tbody>
<tr>
<td>58.3 dB</td>
<td>9.4 bits</td>
<td>±2LSB</td>
<td>±1.8LSB</td>
</tr>
</tbody>
</table>

The chip provides an interface to piezoelectric sensors for dynamic parameter measurement such as angular velocity, pressure, temperature, acceleration and so on.

4.1 Miniature Pressure Measurement System

Pressure measurement is an important component part of mechanics measurement. Most of the tested pressure signal is dynamic variation or impact signal. The signal can be acquired by tiny measurement instrument, which is fixed in tested object. This test method is one of the most reliable, accurate methods for dynamic pressure-testing at present.

Miniature pressure measurement system (MPMS) consists of the miniature pressure tester (MPT) and virtual panel based on PC, which measures the pressure rang of 0-500MPa. MPT includes piezoelectric pressure sensor, single SCIC, trigger switch, high-strength shell etc. and rechargeable battery supplied power. The sensor is selected Kistler 6215BAQ01 fixed point where the pressure is focused on. The sample frequency of this MPT is 100 kHz. After testing, the tester can be taken out and the sampled data can be transferred from memory to PC. The data will be processed or replayed on virtual panel.

In order to validate the performance and accuracy of MPMS, two testing systems should be adopted in the same test condition. One is the high accuracy system which consisted of Kistler 6213BK calibrated sensor and 5015 charge amplifier, the other is MPMS. Fig.10 shows the waveforms tested by these two systems. In this figure, solid and dotted lines stand for tested waveform of MPMS and high accuracy system, respectively. Since the measured signal is acquired in independent test systems, it must have a certain delay τ between the pressure waveform. After the two waveforms are panned through, the dynamic error of MPMS can be evaluated by the analysis of waveforms correlation. Correlation coefficient of these waveforms is 0.99993, relative error energy is 0.014‰.
4.2 Miniature Oil Well Measurement Systems

The dynamic characters, such as pressure and acceleration, are important to study character and master dynamic state of oil-gas layer during the course of perforation or fracturing in prospecting well testing. The varied regulation of these parameters can be acquired automatically and correctly by miniature oil-well measurement system (MOWMS), which is based on SCIC fixed under well. MOWMS is composed of sensors, two SPSICs, virtual panel and others.

Pressure and acceleration have their respective range of 0-210MPa, ±50,000g. Consequently, the sensors adopt Kistler-6213 piezoelectric pressure sensor and CA-YD-111A piezoelectric acceleration sensor. The other channels may monitor temperature and system state, which are reference information for analysis. MOWMS needs a varied sample frequency of 0.5-125kHz and 256K×12bit memory size per parameter. So, the two SCICs are adopted memory cascade model to enlarge the memory size from 128K×12bit to 256K×12bit per channel. The miniature tester based on two SCICs is shown in Fig.11. Fig.12 shows the waveforms of pressure and acceleration in one course of complex perforation.

5. CONCLUSION

In this paper, we proposed a smart cascade interface chip for piezoelectricity sensor, which based on SOC technology and is suitable for MSMS or miniature data acquisition system. This cascade structure can be extended by increasing, reducing the number of integrated chips, convenient and fast way to meet the test requirements. The chip is different from other integrated chips, it will not because of the inherent properties of designed limits its applications. As chip integration of multiple data acquisition modules, so cascade use, the chip requires only two pins for the connection and communication between them. Tests and measurements show
the chip has excellent performance in applications. The flexible combination of many operation modes and parameters can greatly expand application area of SCIC.

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